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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/629,866	07/30/2003	Jae-Jun Lee	SEC.1058	7366
20987	7590	10/05/2006	EXAMINER	
VOLENTINE FRANCOS, & WHITT PLLC ONE FREEDOM SQUARE 11951 FREEDOM DRIVE SUITE 1260 RESTON, VA 20190			KIM, DANIEL Y	
			ART UNIT	PAPER NUMBER
			2185	

DATE MAILED: 10/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/629,866	LEE ET AL.	
	Examiner	Art Unit	
	Daniel Kim	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 07 July 2006.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-11 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-11 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 30 July 2003 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date: _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date: _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

1. This Office Action is in response to applicant's communication filed July 7, 2006 in response to the PTO Office Action mailed May 14, 2006. The applicant's remarks were considered with the results that follow.
2. In response to the last Office Action, no claims have been amended, canceled or added. Claims 1-11 remain pending in this application.
3. Applicant's arguments with respect to claims 1-11 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.
5. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Abe (US PGPub No. 20020142660) and Dong (US Patent No. 6,725,314).

For claim 1, Abe discloses a memory system comprising:

at least one single in-line memory module (SIMM) including at least one memory device and a signal transmission line connected between the memory device and a connection terminal (a plurality of sockets into which a plurality of electronic parts are inserted, a coupling element which connects the sockets together, par. 0007; a connector which includes a plurality of terminals provided in a plurality of holes, wherein the electronic parts are inserted to the holes, a plurality of pins are provided and a wiring network via which the terminals and the pins are connected, par. 0008; where the electronic parts may include different types of memory modules such as a Dual-Inline Memory Module, par. 0020); and

at least one dual in-line memory module (DIMM) including at least two memory devices and a signal transmission line connected between the two memory devices and a connection terminal (par. 0007-0008, 0020).

For claim 1, Abe does not expressly disclose a longer length of the at least one SIMM signal transmission line than that of the at least one DIMM.

Dong, however, discloses memory module connectors are mounted on a motherboard or system board such that the memory modules connect to a memory bus one row after another or in a daisy chain (col. 1, lines 43-46), where some memory modules are closer to the memory controller than the other memory modules (col. 2, lines 15-16), and where two commonly used such memory modules include SIMMs and DIMMs (col. 1, lines 27-29). It could therefore be reasonably assumed that at least one SIMM signal transmission line is of a longer length than that of at least one DIMM.

Abe and Dong are analogous art in that they are in the same field of endeavor, that is, a system for memory arrangement. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include differing lengths of transmission line because this is a common design choice in many systems for arranging memory modules (col. 1, lines 43-46), as taught by Dong.

6. Claims 2, 4 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abe (US PGPub No. 20020142660), Dong (US Patent No. 6,725,314) and Doblar et al (US PGPub No. 20030043613).

For claim 2, the combined teachings of Abe and Dong disclose the invention as per rejection of claim 1 above.

These teachings do not expressly disclose that the load of the at least one memory device of the at least one SIMM is less than the load of the at least one DIMM.

Doblar, however, discloses that the total load on a signal driver includes the sum of the chip inputs connected to the line (par. 0006), and that SIMMs have opposing contact pads are connected together (i.e. shorted), and thus carry the same signal, while at least some of the opposing contact pads on DIMMs are not connected, thus allowing different signals to be carried (par. 0005).

Abe, Dong and Doblar are analogous art in that they are in the same field of endeavor, that is, improvement upon signal transmission in memory systems. It would have been obvious to a person of ordinary skill in the art at the time of the invention that the load of memory devices of a SIMM are less than the load of memory devices on a

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DIMM because a DIMM has a greater sum of contact pads, or equivalently, chip inputs, which result in a greater load (par. 0005-0006), as taught by Doblar.

For claim 4, the combined teachings of Abe, Dong and Doblar as per rejection of claims 1-3 are incorporated herein.

These teachings further help disclose a memory controller (Dong: col. 2, lines 15-16);

a first memory module including at least one first memory device having a first load and a first signal transmission line connected between the at least one first memory device and a connection terminal (Abe: par. 0007-0008; Dong: col. 2, lines 15-16; Doblar: par. 0005-0006);

a second memory module including at least one second memory device having a second load and a second signal transmission line connected between the at least one second memory device and a connection terminal, wherein the second load is greater than the first load (Abe: par. 0007-0008; Dong: col. 2, lines 15-16; Doblar: par. 0005-0006); and

first and second sockets which are connected to the memory controller and which respectively receive the connection terminals of the first and second memory modules (Abe: par. 0007-0008; Dong: col. 2, lines 15-16; Doblar: par. 0005-0006),

wherein a length of the first signal transmission line of the first memory module is longer than a length of the second signal transmission line of the second memory module (Abe: par. 0007-0008; Dong: col. 2, lines 15-16; Doblar: par. 0005-0006).

For claim 8, the combined teachings of Abe, Dong and Doblar as per rejection of claim 4 further help disclose the first memory module is a single in-line memory module, and the second memory module is a dual in-line memory module (Dong: col. 1, lines 27-29).

7. Claims 3, 5-7 and 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abe (US PGPub No. 20020142660), Dong (US Patent No. 6,725,314), Doblar et al (US PGPub No. 20030043613), Ono et al (US PGPub 20020041020) and Dixon et al (US Patent No. 6081862).

For claim 3, the combined teachings of Abe, Dong and Doblar disclose the invention as per rejection of claim 2 above.

These teachings do not expressly disclose the longer length of the signal transmission line of the at least one SIMM increases the signal delay time of the at least one SIMM to further compensate for the signal delay time difference caused by the signal transmission line connected between the first and second sockets.

Ono, however, discloses that in a bus having multiple slots, the degree of influence to the waveforms that the reflected waves give at the termination greatly differs at the socket near side or at the socket far side, and, as the number of the sockets increases, the length of the bus wiring becomes longer, and the wiring capacity (and equivalently, load) increases, therefore, a shorter bus wiring with a shorter distance between the sockets in addition will achieve a better characteristic (par. 0009).

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Abe, Dong, Doblar and Ono are analogous art in that they are in the same field of endeavor, that is, improvement upon signal transmission in memory systems. It would have been obvious to a person of ordinary skill in the art at the time of the invention that a longer length of the signal transmission line of a SIMM increases the signal delay time of the SIMM to compensate for the transmission line connected between sockets because wiring between sockets increases load, and adjusting the length of the signal transmission lines is one method of compensating for differing delay times and loads (col. 1 lines 66-67 and col. 2 lines 1-4), as taught by Dixon.

For claim 5, the combined teachings of Abe, Dong, Doblar, Ono and Dixon as per rejection of claims 3-4 are incorporated herein.

These teachings further help disclose the longer length of the first signal transmission line of the first memory module increases a signal delay time of the first memory module to compensate for the different loads of the first and second modules (Abe: par. 0007-0008; Dong: col. 2, lines 15-16; Doblar: par. 0005-0006; Ono: par. 0009; Dixon: col. 1 lines 66-67 and col. 2 lines 1-4).

For claim 6, the combined teachings of Abe, Dong, Doblar, Ono and Dixon as per rejection of claim 5 further help disclose a third signal transmission line connected between the memory controller and the first socket, and a fourth signal transmission line connected between the first socket and the second socket, wherein the longer length of the first signal transmission line of the first memory module further compensates for the signal delay time difference caused by the fourth signal transmission line connected

between the first and second sockets (Abe: par. 0007-0008; Dong: col. 2, lines 15-16; Doblar: par. 0005-0006; Ono: par. 0009; Dixon: col. 1 lines 66-67 and col. 2 lines 1-4).

For claim 7, the combined teachings of Abe, Dong, Doblar, Ono and Dixon as per rejection of claim 6 further help disclose each of the first, second and third signal transmission lines includes an impedance matching resistive element (Abe: wires are constructed such that they have an impedance equal or close to that of the printed circuit board, par. 0027; fig. 4, items 1111-1117, 300).

For claim 9, the combined teachings of Abe, Dong, Doblar, Ono and Dixon as per rejection of claim 5 further help disclose the first memory module is a single in-line memory module, and the second memory module is a dual in-line memory module (Dong: col. 1, lines 27-29).

For claim 10, the combined teachings of Abe, Dong, Doblar, Ono and Dixon as per rejection of claim 6 further help disclose the first memory module is a single in-line memory module, and the second memory module is a dual in-line memory module (Dong: col. 1, lines 27-29)

For claim 11, the combined teachings of Abe, Dong, Doblar, Ono and Dixon as per rejection of claim 7 further help disclose the first memory module is a single in-line memory module, and the second memory module is a dual in-line memory module (Dong: col. 1, lines 27-29)

Citation of Pertinent Prior Art

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Woo et al (US PGPub No. 20050262323) discloses a memory system where memory may reside at different electrical distances from a memory controller, resulting in different times of flight for signals between the memory devices and memory controller.

Contact Information

9. Any inquiries concerning this action or earlier actions from the examiner should be directed to Daniel Kim, reachable at 571-272-2742, on Mon-Fri from 10:00am-6:30pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah, is also reachable at 571-272-4098.

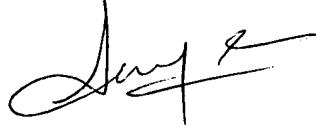
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